RF Synthesizers: PLL switching speed and speed-up techniques A short review

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ABSTRACT — **Traditionally, designers of frequency synthesizers, especially for high volume wireless applications, are mainly focused on the improvement of phase noise and noise floor of signals, always a fundamental property and a constant challenge in the design of radio and wireless networks.**
Recently, switching speed has become a critical parameter in the design of PLL synthesizers too, especially for 3G, WCDMA, WLAN and future generations of mobile, high data rate and complex wireless networks. High resolution, fast hopping, economical (size, cost, power) single loop synthesizers not compromising spectral purity, are a recent possibility. Only the combination of RF, digital and DSP (Fractional and Delta Sigma type) PLL technologies can offer this capability, as a networking and spread spectrum (combating multipath/fading) technique. The purpose of this article/presentation is to briefly review PLL switching speed issues and speed up mechanisms. Special focus will be given to CAD simulation results, optimization and view on strength, limitations, and future trends.

PLL Synthesizers

PLL synthesizers are a fundamental block in every radio and timing device, for their utility, simplicity and great economy. Most analysis and the calculation of loop dynamics and transfer functions are done assuming that the loop is linear.
This assumption is quite accurate, or at least justified, especially for narrow band wireless systems where the VCO constant, Kv, and phase detector constant Kp, are fix values. When locked, PLL can certainly be modeled as a linear system (though phase detector non linearity will be analyzed in another lecture). Loops are usually analyzed as extension of the basic 2nd order, with practical applications using 3rd, 4th and 5th order loops, as necessary. Basic loop transfer function is given by: $H(s)=N\bullet OL(s)/1+OL(s)$, where OL(s) is the open loop transfer function; generally for a 2nd order loop with natural frequency wn and damping factor ξ, $H(s)=N\bullet(2wn\xi s+wn^2)/s^2 + 2wn\xi s+wn^2$

Most loops used for synthesizers are 3rd or 4th order, with passive loop filter structure as shown when using a charge pump.

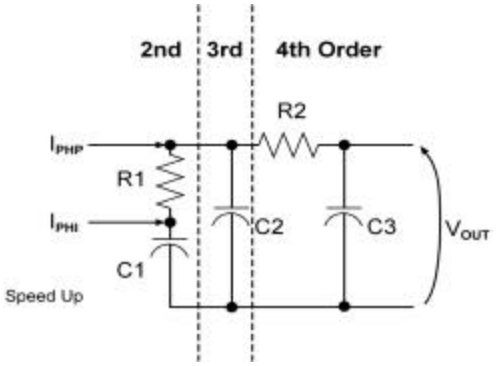

Figure 1:Loop filter with speed up current. Current can be pumped as shown or added to Iphp, see details later.

Switching speed

Switching speed in PLL is complex to analyze and simulate. The PLL phase detector (PFD) is operating as a sampling device (phase is measured once per reference cycle) and is linear only in the range +/- 2π, hence switching transient is subject to non linear behavior that complicates the analysis. Other parameters might not be linear either.
The approximate time solution of the 2nd order linear loop, yields the well known equation:

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$df \sim dF \bullet e^{-wn\xi t}$, where dF is the hop size, and df the required resolution.
In synthesizers $\xi \sim 1$. Hence: $Tsw \sim \ln(dF/df)/wn$.
Our practical experience shows that the approximation $Tsw=k \bullet \ln(dF/df)/wn$ fits experimental results better, $1<k<2$.
This equation shows only the obvious: speed is inversely proportional to loop bandwidth (and logarithmically to the excursion dF). Therefore, the two obvious methods to improve speed is by widening the loop or decreasing frequency excursion. These however are not always possible due to conflicting requirements from other synthesizer parameters, mainly spectral purity.

Simulation Tools

Generally, switching analysis can be done by either using time domain analysis tools (Spice type) or stay in the Laplace frequency domain and use Inverse Laplace transform.
Spice, which is more detailed, has to take into consideration the phase frequency detector transfer function, as shown below, while Inverse Laplace usually assumes a linear loop.

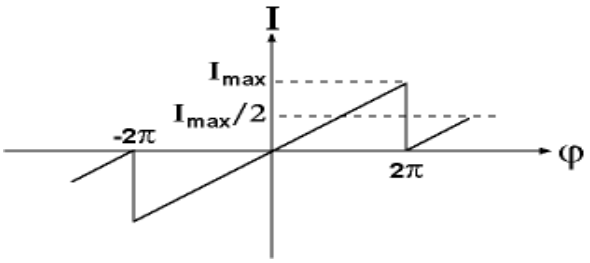
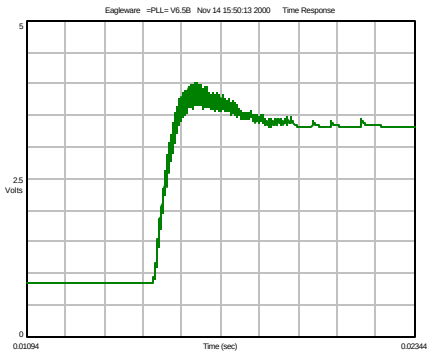


Figure 2: Phase Frequency Detector typical transfer function

Typical Spice run is shown below. Frequency has been commanded to change by 25MHz. The loop is quite optimized, with no oscillations before settling. Jagged line indicates the charge and discharge of C2 to C1 until eventual lock. Remember that C2<<C1.



A similar Inverse Laplace transform analysis is shown below (Figure 3), having same characteristics but less per sample details.
This plot uses Mathcad as simulation platform.
Another interesting plot is to view the instantaneous PFD phase error, and check if we exceed the linear region (not shown).

Speed up mechanisms

As mentioned, the two fundamental parameters concerning speed are dF (frequency excursion) and wn, loop bandwidth.
The only way to effect dF is by pre-tuning the VCO, using some type of look up table. My experience is that it is most effective and can be

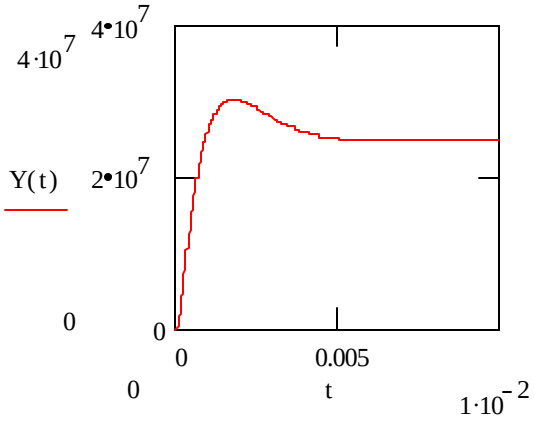


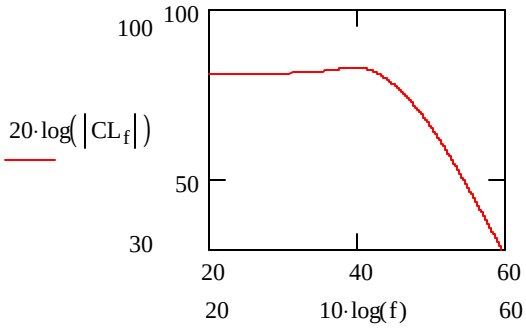
Figure 3: speed simulation

adapted to on chip design easily, however it's not simple or popular yet.
All other speed up use techniques to increase loop bandwidth for a short time, to speed up the acquisition time.
It is easy to show that loop bandwidth is proportional to KvKpR/N, where Kv and Kp are

VCO and CP constants, R is the 2nd order resistor and N division ratio.
Open loop gain for 2nd order loop is given by: $KvKp(1+sCR)/s^2 NC$. The absolute value of this term is 1 when the open loop slope goes from –12 to –6 dB/decade (stability condition), hence the numerator zero is active and OL can be approximated by $KvKpsCR/s^2 NC$, hence the crossover frequency wp, is approximately:
$wp \sim KvKpR/N$.

The following parameters can be changed to effect loop bandwidth:
1.Kp can be increased – this is done by applying another charge pump, similar to the main one, thus adding current for a specific time, usually controlled by the serial interface.
N can be decreased – simultaneous decrease in the value of main divider N and reference divider R. Remember that Fo=NFr=NFx/R, (Fx is xtal frequency), if N and R are decreased by the same amount, phase lock will still attempt to lock to the right frequency but loop bandwidth will increase.
Resistor value R can be increased – not very practical.

All speed up technique must be performed for an optimized time (a look up table can be easily generated to decide how long the speed up is active) and must be performed while the loop is stable. The most common speed up, increase in Kd, can be stabilized by reducing resistor value R, as shown in the figure below, and providing an analog switch that enables reducing value R for the speed up time. For example, by increasing the charge pump current, the loop becomes wider, see below for 8 times increase, but also "oscillatory".
Generally, decreasing the value of R, insures loop stability. Loop parameters must be optimized for switching too, just increasing bandwidth will not do the trick alone.



Conclusion and challenges

Switching speed in PLL synthesizer is becoming a fundamental requirement for use as a networking as well as mechanism for combating multipath/fading. Until recently, PLL circuits used mainly Integer architecture, however the introduction of fractional circuits, especially 3rd order (Sigma Delta) enable the use of a very high reference frequency, good phase noise performance and significant improvements in switching speed as loops become wider and speed up mechanisms improve.

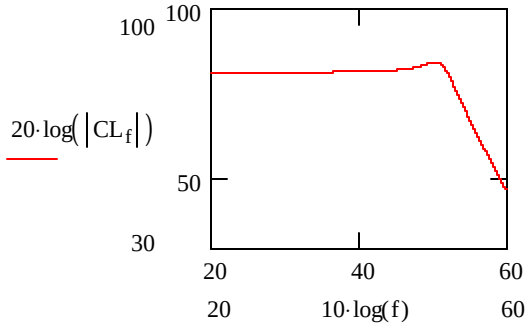
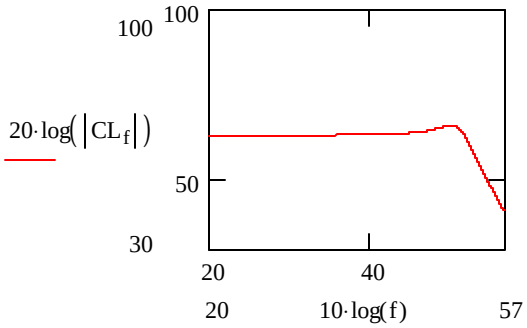
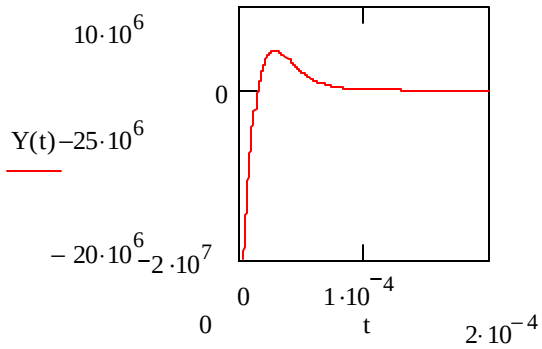


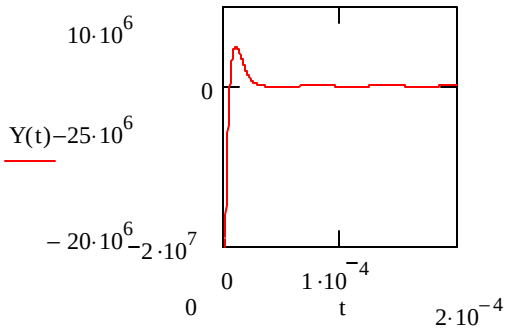
Figure 4: Close loop change for changing Kp by 8:1 Same with changing N by 8:1, in comparison to previous plot is shown below.



Comparison between transient for nominal N:

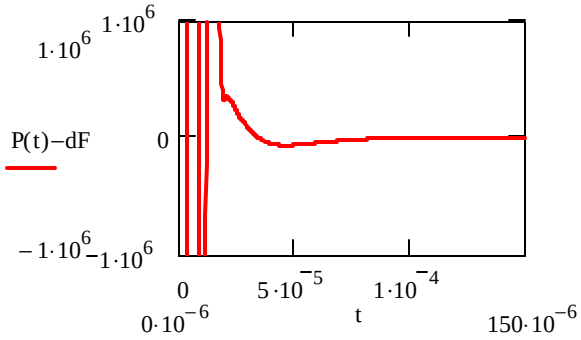


and N/8:



R was adjusted somewhat to compensate for change in transfer function “stability”.

Speed up simulation:
Note the loop transient change after 20usec.



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